

OCT 03 2005

09/867,766

REMARKS

Claims 1 and 5 stand rejected under 35 U.S.C. § 112, second paragraph. It is respectfully submitted that the enclosed amendment obviates the alleged indefiniteness ("address by address" can embody "mutually different addresses"). Accordingly, it is respectfully requested that this rejection be withdrawn.

Claims 1 and 5 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hartung et al. in view of Applicants' admitted prior art ("APA"), or over Hartung et al. in view of Katsuta et al.. These rejections are respectfully traversed for the following reasons.

In order to expedite issuance of the present application, the features recited in claims 2-3 have been added into claims 1 and 5 (not new issue, so entry for purposes of appeal is respectfully requested) without prejudice/disclaimer to the subject matter embodied by claims 1 and 5.

Each of claims 1 and 5 embody the storage device being included in the ROM, wherein the plural redundancy check data and each of the corresponding plural confidential data are stored at mutually different addresses on the ROM. In direct contrast, Hartung, which the Examiner relied on as allegedly disclosing the aforementioned features, discloses that the 4,096 byte data block is stored in registers represented by the address space 21 whereas the CRC is stored in registers 22 (*see* Fig. 2 and col. 3, lines 38-55).

According to the present invention, plural confidential data can be stored on a ROM and plural redundancy check data can be stored in a storage device *which is included in the ROM*. Accordingly, both confidential data and redundancy check data can be stored on the ROM, whereby the area per bit can be made smaller than that of Hartung.

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Each of claims 1 and 5 also embody a ROM that stores plural confidential data thereon address by address which cannot be read out from the integrated circuit. In direct contrast, Katsuya discloses *external* input data is read out from the input port 5, and the key data is also read, so that the external input data and the key data #1 are compared (*see* col. 4, lines 15-18). Moreover, all contents of the ROM 4 including the user program area are read out, and the read-out data is transferred or written to the output port 6 (*see* col. 4, lines 34-37). Turning to Hartung, the CRCG 50 sends the accumulated CRC 22 via bus 63 to bus 13 for recording in data storage unit 10 (*see* col. 6, lines 61-64).

According to the present invention, confidential data and redundancy check data can be stored on the ROM which cannot be read from outside of the integrated circuit, whereby the data security level can be made higher than that of Katsuya and Hartung.

In view of the foregoing, it is respectfully submitted that none of the cited prior art, alone or in combination, disclose or suggest the claimed combination of features recited in claims 1 and 5. The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard for establishing obviousness under § 103:

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejections do not "establish *prima facie* obviousness of [the] claimed invention" as recited in claims 1 and 5 because the proposed combinations fail the "all the claim limitations" standard required under § 103.

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Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. § 103 be withdrawn.


CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



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WDC99 1142108-1.060188.0075

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Docket No.: 060188-0075

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Customer Number: 20277
Makoto FUJIWARA : Confirmation Number: 5700
Application No.: 09/867,766 : Group Art Unit: 2134
Filed: May 31, 2001 : Examiner: Poltorak, Piotr
For: SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD OF TESTING
SEMICONDUCTOR INTEGRATED CIRCUIT

REQUEST FOR ACKNOWLEDGEMENT OF THE CITED ART

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reviewing the file, it is noted that we have not received acknowledgement of the Information Disclosure Statement and cited art U.S. Patent No. 6,006,354 and U.S. Patent No. 4,905,142, filed May 31, 2001. Enclosed are copies of the Information Disclosure Statement, PTO-1449 and stamped return postcard acknowledgement.

Applicant hereby respectfully requests that:

- (1) the appropriately acknowledged PTO-1449 be furnished to Applicant; and
- (2) the record be clarified to confirm that the cited art has been considered and made of record.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

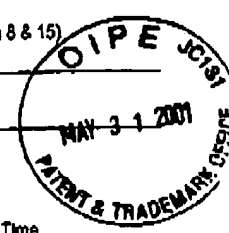
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Date: October 3, 2005

Applicant: <u>Makoto FUJIWARA</u>		Docket No. <u>60188-075</u>	
Title/Mark: <u>SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD OF TESTING SEMICONDUCTOR INTEGRATED CIRCUIT</u>		Serial/Reg./Patent No. <u>NOT YET ASSIGNED</u>	
Date Sent: <u>May 31, 2001</u>	<input checked="" type="checkbox"/> Hand Carried	<input type="checkbox"/> Fax	<input type="checkbox"/> Electronic
<input checked="" type="checkbox"/> Transmittal Letter		<input type="checkbox"/> Cert. of Mailing	<input type="checkbox"/> Express Mail No. _____
New Patent App	<input checked="" type="checkbox"/> Utility	<input type="checkbox"/> Design	<input type="checkbox"/> Cont.
<input checked="" type="checkbox"/> Other:	<input type="checkbox"/> CIP	<input type="checkbox"/> Div.	<input type="checkbox"/> PCT
<u>12</u> pages of Specification	<input type="checkbox"/> CPA	<input type="checkbox"/> RCE	<input type="checkbox"/> Prov
<u>2</u> pages of Claims	<input type="checkbox"/> Trademark/Service Mark/Intent-To-Use Application	<input type="checkbox"/> Statement of Use	
<u>1</u> pages of Abstract	<input type="checkbox"/> Amendment to Alleged Use	<input type="checkbox"/> Formal/Informal/Substitute Drawing Sheet	
<u>4</u> pages of Formal/Informal Drawings	<input type="checkbox"/> (no. of) Substitute/Specimens	<input type="checkbox"/> Continued Use Affidavit/Declaration (Section 8 & 15)	
<input checked="" type="checkbox"/> Information Disclosure Statement	<input type="checkbox"/> Notice of Opposition/Answer to	<input type="checkbox"/> Ex Parte Appeal	
<u>1</u> Form PTO 1449	<input type="checkbox"/> Petition for Cancellation/Answer To	<input type="checkbox"/> Renewal of Reg. No.	
<u>2</u> copies of cited references	<input type="checkbox"/> Combined Declaration/Power of Attorney	<input type="checkbox"/> Letter of Protest	
<input type="checkbox"/> Preliminary Amendment	<input type="checkbox"/> Request for _____day/month Extension of Time	<input type="checkbox"/> Request for Non-Publication	
<input type="checkbox"/> Response to Missing Parts Notice	Assignments/Security Agreements/		
<input type="checkbox"/> Certified Copy of Priority Doc	<input type="checkbox"/> Petition to Commissioner for		
<input checked="" type="checkbox"/> Claim for Convention Priority			
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THE PATENT AND TRADEMARK OFFICE DATE STAMPED HEREON IS ACKNOWLEDGEMENT THAT THE ITEMS, CHECKED ABOVE, WERE RECEIVED BY THE PTO ON THE DATE STAMPED.								

Docket No.: 60188-075

PATENT**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of

Makoto FUJIWARA

Serial No.:

Group Art Unit:

Filed: May 31, 2001

Examiner:

For: SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD OF TESTING
SEMICONDUCTOR INTEGRATED CIRCUIT**INFORMATION DISCLOSURE STATEMENT**Commissioner for Patents
Washington, DC 20231

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits.

WDC99 442022-1 043890 0010

No certification or fee is required.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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WDC99 442022-1.043890.0010

SHEET 1 OF 1

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)				ATTY. DOCKET NO. 60188-075		SERIAL NO.	
				APPLICANT Makoto FUJIWARA			
				FILING DATE May 31, 2001		GROUP	
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
	4,905,142	FEB. 27, 1990	MATSUBARA, ET AL.				
	6,006,354	DEC. 21, 1999	MCGUINNESS				
FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER				DATE CONSIDERED			

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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